Applicant whether the Office action is taking the position that the argued claim limitation is identically shown in the De Natale reference, or whether the claim limitation is considered to be obvious in light of the De Natale reference (given that the quoted language includes the phrase "would").

However, at page 3 of the Office action it is indicated that ". . .the top view is dependent on the orientation of the device or the person." Thus, in light of this statement it appears that the Office action is taking the position that Fig. 7 of the De Natale reference is a "top" view. Under this interpretation the upper wafer portion (50, 60, 70) would be considered to define a coverage area (i.e., a rectangular box in Fig. 7) and the solderable surface (believed to be construed by the Examiner as the contacts 82 (Fig. 6) located immediately above the contacts 94, 98 and/or 99 (Fig. 7)) is not located within the "coverage area."

However, it is submitted that such an interpretation is clearly not supported by the De Natale reference. More particularly, at column 4, line 25, De Natale specifically indicates that Fig. 7 is a "sectional view." In addition, Fig. 7 of De Natale is shown as a side cross section, as indicated by the cross hatching of the layers of Fig. 7. Thus, Fig. 7 of De Natale is an internal sectional view, which cannot even be seen without forming a section or cutting away part of the De Natale device.

As can be seen in Fig. 10, the device of the De Natale reference is a generally flat, planar component. It is submitted that one of ordinary skill would understand that a "top" view of a generally flat, planar component (such as the upper wafer portion) would be a view taken perpendicular to the plane of the flat, planar component (i.e., looking down on the plane). Indeed, throughout Applicant's specification, a top view is repeatedly and consistently referred to as a view taken from this perspective.

For example, at page 3, line 6 of this application, it is disclosed that Fig. 2 is a top plan view, which can be seen to be a top view in the manner described above. At page 9, lines 3-6, the application describes placing contacts 83 on "top" of the connection sites 81 in a manner consistent with this interpretation of a top view. At page 10, lines 8-13, the term "coverage area" is defined with reference to a "top view" as indicated in Fig. 2. In contrast, Figs. 6 and 7 of the application are indicated to be cross sections, and those figures are analogous in view of Fig. 7 to De Natale. Finally, claim 28 specifies that the wafer portion includes an upper wafer portion and

a lower wafer portion, thereby inherently defining a sense of direction in that claim consistent with this interpretation. Thus, the terminology and conventions used in the specification and claim of this application are entirely consistent with those indicated and specified in the De Natale reference, as contrasted with the interpretation that appears to be taken in the Office action.

In addition, claim 32 depends from claim 28 and specifies that the lower wafer portion has a coverage area in top view, and that the coverage area of the upper wafer portion is "entirely contained within" the coverage area of the lower wafer portion. Under the interpretation believed to be taken in the final Office action, claim 32 would carry no meaning since an upper wafer portion that is "entirely contained within" a coverage area of the lower wafer portion in side cross section is no longer an "upper" wafer portion, but is instead coincident with or entirely contained within the "lower" wafer portion.

As noted in Applicant's previous Amendment, providing a solderable surface that is outside the coverage area provides certain advantages during manufacture and use of the microstructure. As noted at page 10, second full paragraph of this application, locating each of the connection sites 88/solder pads 80 outside of the coverage area of the upper wafer allows of the connection sites 88 to be easily accessed. For example, as shown in Fig. 7 of this application, the solder pads 80 are not located within the coverage area of the upper wafer 34, but are laterally offset therefrom. As shown in Fig. 8, this arrangement allows a chip 81 to be easily coupled to the connection site 88 from a front side of the mirror array. In contrast, in the De Natale reference, the only way in which the contacts 82 of Figs. 6 and 7 can be accessed is from the underside of the mirror array.

In the rejection of claim 50, the Office action indicates that it would have been obvious to have an upper wafer area smaller than the lower wafer area in order to "provide an additional space/substrate wherein an additional element can be connected." However, in this case it is submitted that the Office area has used the Applicant's disclosure as a template to interpret the prior art. The application, for example, at page 10, lines 14-16, specifies that "Each of the connection sites 88 may be located on the underhang portion 87 to ensure that the connection sites 81 can be easily accessed to enable a chip 81 to be easily coupled to each connection site 88." MPEP §2145 notes that "any judgment on obviousness is in a sense reconstruction based on

hindsight reasoning, but so long as it . . . *does not include knowledge gleaned only from Applicant's disclosure* such a reconstruction is proper." In this case, the Office action appears to use an identical benefit cited in this Application as a motivation for modifying the prior art.

Thus, in sum, it is submitted that the De Natale reference does not disclose or suggest a solderable surface formed or located on the lower wafer portion and not located within the coverage area, wherein the coverage area is defined by an upper view of the upper wafer portion. Accordingly, it is submitted that claim 28 is patentable over the De Natale reference. Independent claims 56 and 118 include limitations analogous to those discussed above, and are also therefore submitted to be allowable.

Claims 56, 118 and 122 include as a claim element an electronic component coupled to the microstructure/solderable surface. Claim 56 specifies that the electronic component is generally not located within the coverage area of the upper wafer portion. Claim 118 specifies that the electronic component is coupled by flip chip bonding. Claim 122 specifies that the electronic component is positioned generally between the upper and lower wafer portions.

Upon a review of the Office action, it is unclear to Applicant exactly which component the Office action has construed as the claimed electronic component. In some cases (i.e., page 2 of the Office action), the element 66 of De Natale appears to be construed as the claimed electronic component. The Office action later (at page 4) construes the element 66 as a claimed electrode (which is different from the electronic component) in the context of claims 45-47. However, even if the element 66 is construed as the claimed electronic component, the element 66 of De Natale is clearly not outside the coverage area of the upper wafer portion, even under the Office action's apparent interpretation of the claimed coverage area. The element 66 is also not positioned between the upper and lower wafer portions.

In any case, the claimed electronic component does not appear to be shown. Thus, it is submitted that claims 56, 118 and 122 also define over the De Natale reference for this reason.

Claim 40 depends from claim 28 and specifies that the electronic component is a chip, thereby further distinguishing over the De Natale reference.

Dependent claim 113 depends from claim 28 and specifies that the upper wafer portion and lower wafer portion are coupled together by an electrically insulating material such that the upper and lower wafer portions are not directly electrically connected. At page 7 the final Office

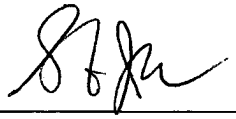
action takes the position that it would have been obvious to have an electrically insulating material between the upper and lower wafers in order to prevent unwanted electrical signals from inadvertently passing between the wafers.

However, it is submitted that the De Natale reference specifically teaches against this proposed modification. In particular, electrical signals are required to be passed between the two wafers of De Natale in order for that device to function as desired. With reference to Fig. 7, electrical signals are passed from the drive electronics 92 to the upper wafer portion 50, 60, 70 via the contacts 94, 98, 99. If the upper wafer portion 50, 60, 70 were to be electrically insulated from the lower wafer portion 92, then no electrical signals could pass and all function and utility of the De Natale reference would be destroyed.

At column 6, lines 20-22 of De Natale, it is specified that the structure is mechanically and *electrically* attached to the substrate with drive electronics utilizing flip chip bonding, with this electrical attachment being necessary for the reason outlined above. In addition, in the rejection of claim 120, the Office action takes the position that it would be obvious "to have placed a solderable surface on the upper surface of the lower wafer portion in order to connect/join the lower wafer portion with the upper wafer portion *in order for the system to communicate*" (emphasis added). Thus, the rejection of claim 120 recognizes the importance of communication between the upper and lower wafer portions, and appears to contradict the statements with respect to claim 113. Thus, it is submitted that claim 113 further distinguishes over the De Natale reference. Claim 119 depends from claim 118 and includes similar limitations.

Thus, in sum, it is submitted that the De Natale reference clearly does not disclose claim features of the independent claims, and at least several dependent claims specifically addressed herein. Thus, it is submitted that the Application is in a condition for allowance, and formal notice thereof is respectfully solicited.

Respectfully submitted,



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